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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,589	05/20/2004	Adam William Saxler	5308-412	6346

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EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/849,589	SAXLER, ADAM WILLIAM	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above claim(s) *11-13,26-45,55-57 and 69-88* is/are withdrawn from consideration.

5)☒ Claim(s) *18-25* is/are allowed.

6)☒ Claim(s) *1-7,46-51 and 61* is/are rejected.

7)☒ Claim(s) *8-10,14-17,52-54,58-60 and 62-68* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/26/4, 8/30/04, 10/25/04, 1/27/05, 6/16/05, 7/5/05, 7/29/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species I (Claims 9, 10, 18-25, 53, 54, and 61-68) in the reply filed on 10/03/2005 is acknowledged. As indicated in the restriction requirement, claims 1-8, 14-17, 46-52 and 58-60 are generic to Species I.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims **61-68** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim **61** recites the limitation "the first conformal layer" in the last line. There is insufficient antecedent basis for this limitation in the claim. The claim is interpreted as if the drain contact was formed on the substrate.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **1-5 and 46-49** are rejected under 35 U.S.C. 102(a) as being anticipated by Ben Yaacov et al.

Regarding claim **1**, Ben Yaacov discloses in Figure 1(a) a transistor comprising a source contact, a drain contact and a gate contact, and a channel region between the source and drain contacts at least a portion of which comprises a hybrid layer comprising semiconductor material. The channel region disclosed by Ben Yaacov comprises an insulating layer containing a narrow aperture that is filled with conducting material, which is interpreted as a hybrid layer.

Regarding claim **2**, Ben Yaacov discloses in Figure 1(a) the transistor of claim 1, wherein the transistor comprises a current aperture transistor.

With regards to claim **3**, Ben Yaacov discloses in the caption of Figure 1(a) the transistor of claim 2, wherein the hybrid layer comprising semiconductor material comprises a Group III-nitride semiconductor material (GaN based).

Regarding claim **4**, Ben Yaacov discloses in Figure 1(a) the transistor of claim 2, wherein the hybrid layer comprising semiconductor material comprises a region comprising insulating semiconductor material (Insul GaN) and a lateral region comprising n-type semiconductor material (UID GaN, described pg. 2073 col 2 ln 5).

With regards to claim **5**, Ben Yaacov discloses in Figure 1(a) the transistor of claim 2, wherein a portion of the channel region through the current aperture comprises a vertical portion and a horizontal portion (lines and arrows show the current path).

Regarding claim **46**, Ben Yaacov discloses in Figures 2(a) – 2(c) a method of fabricating a transistor comprising: forming a channel region at least a portion of which comprises a hybrid layer comprising semiconductor material; and forming a source contact, a drain contact and a gate contact, wherein the channel region is between the source and drain contacts.

With regards to claim **47**, Ben Yaacov discloses in Figure 2(c) the method of claim 46, wherein the hybrid layer comprising semiconductor material comprises a Group III-nitride semiconductor material (GaN:Mg and UID GaN).

Regarding claim **48**, Ben Yaacov discloses in Figure 2(c) the method of claim 46, wherein forming a channel region at least a portion of which comprises a hybrid layer comprising semiconductor material comprises forming a hybrid layer comprising a region comprising insulating semiconductor material (GaN:Mg) and a region comprising n-type semiconductor material (UID GaN).

With regards to claim **49**, Ben Yaacov discloses in Figure 2(c) the method of claim 46, wherein a portion of the channel region through the current aperture comprises a vertical portion and a horizontal portion (arrows show the current path).

6. Claims **1, 2, 4, 6, 7, 46, 48, 50, and 51** are rejected under 35 U.S.C. 102(e) as being anticipated by Howard (US 2005/0006663).

Regarding claim **1**, Howard discloses in Figure 2 a transistor (10) comprising a source contact (450), a drain contact (150) and a gate contact (320) and a channel

region (350, 310, 210) between the source and drain contacts at least a portion of which comprises a hybrid layer comprising semiconductor material (layer 200).

Regarding claim **2**, Howard discloses in Figure 2 the transistor of claim 1, wherein the transistor comprises a current aperture transistor (aperture formed by SiN 420, p type areas 210 and 310, and dielectric 220).

With regards to claim **4**, Howard discloses in Figure 2 the transistor of claim 2, wherein the hybrid layer comprising semiconductor material (200) comprises a region comprising p-type material (210) and a lateral region (350) comprising n-type semiconductor material.

Regarding claim **6**, Howard discloses in paragraph 22 that element 210 of layer 20 (Figure 2) is substantially p-type silicon, formed by epitaxy. The vertical channel region (350), as disclosed in paragraph 23, is formed by implanting n-type ions into element 210. Therefore, the limitations of claim 6 are met, wherein the hybrid layer (200) comprises an epitaxial layer having a higher doping level in the *channel region*. The claim language "pendeo-epitaxial" is considered product by process, determination of patentability is based on the product itself. See MPEP 2113. The hybrid layer/channel region of Howard is interpreted as being equivalent to pendeo-epitaxial layer.

Regarding claim **7**, Howard discloses in paragraph 22 that element 210 of layer 20 (Figure 2) is substantially p-type silicon, formed by epitaxy. The vertical channel region (350), as disclosed in paragraph 23, is formed by implanting n-type ions into element 210. Therefore, the limitations of claim 7 are met, wherein the hybrid layer

(200) comprises an epitaxial overgrown layer having a higher doping level in the *channel region*. The claim language "laterally overgrown" is considered product by process, determination of patentability is based on the product itself. See MPEP 2113. The channel region of Howard is interpreted as being equivalent to applicant's laterally grown portions of the epitaxial laterally overgrown layer.

Regarding claim **46**, Howard discloses in Figures 3-7 a method of fabricating a transistor comprising: forming a channel region (350, 310, 210) at least a portion of which comprises a hybrid layer (210-350) comprising semiconductor material; and forming a source contact (450), a drain contact (150) and a gate contact (320), wherein the channel region is between the source and drain contacts.

Regarding claim **48**, Howard discloses in Figures 3-7 the method of claim 46, wherein forming a channel region at least a portion of which comprises a hybrid layer comprising semiconductor material comprises forming a hybrid layer comprising a region comprising p-type semiconductor material (210, 310) and a region comprising n-type semiconductor material (350).

With regards to claim **50**, Howard discloses in Figures 3-7 the method of claim 46, wherein forming a channel region between the source and drain contacts at least a portion of which comprises a hybrid layer comprising semiconductor material comprises epitaxially growing a layer (¶ 22) having a higher doping level in the laterally grown portions of the epitaxial layer (350). The method for forming a layer through pendeo-epitaxy is interpreted as equivalent with the method of epitaxy itself.

With regards to claim **51**, Howard discloses in Figures 3-7 the method of claim 46, wherein forming a channel region between the source and drain contacts at least a portion of which comprises a hybrid layer comprising semiconductor material comprises forming a layer using epitaxial overgrowth (¶ 22), the epitaxially overgrown layer having a higher doping level in the laterally grown portions of the epitaxial layer (350). The method for forming a layer through lateral epitaxy is interpreted as equivalent with the method of epitaxy itself.

Allowable Subject Matter

7. Claims **8-10 and 14-17** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not disclose the structure of claim 8 in totality. Claims 9-10 and 14-17 depend from claim 8. Ben Yaacov teaches the creation of current aperture transistors, but not multiple nitride layers filling the aperture nor multiple nitride layers atop the UID layer.

8. Claims **18-25** are allowed. Regarding claim 18, the prior art does not teach a transistor with three layers of cantilevered pendeo-epitaxial material along with a trenched substrate and barrier layer. Claims 19-25 depend from claim 18 and thus are also allowable.

9. Claims **52-54 and 58-60** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Regarding claim 52, the prior

art does not teach the method of creating a transistor with a channel region comprising five nitride-based layers arranged in and above the aperture. Claims 53-54 and 58-60 depend from claim 52.

10. Claims **61-68** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. Regarding claim 61, the prior art does not teach the method of creating a transistor with three layers of cantilevered pendeo-epitaxial material along with a trenched substrate and barrier layer. Claims 62-68 depend from claim 61.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Linthicum teaches lateral pendeo-epitaxy utilizing apertures, but does not create a transistor or provide motivation to do so. Follstaedt teaches cantilever epitaxial growth over substrate trenches, but also does not create transistors. Kidoguchi teaches a technique of air-bridged lateral epitaxy. Wang teaches lateral epitaxy within a substrate trench.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jci

GEORGE ECKERT
PRIMARY EXAMINER